WHAT IS CLAIMED IS:

1. A thin film transistor array panel for a liquid crystal display comprising:

a transparent insulating substrate;

a gate wire formed on the insulating substrate;

a gate insulating layer covering the gate wire;

a pixel electrode formed on the gate insulating layer; and

a data line formed on the gate insulating layer and electrically connected to the pixel electrode.

wherein the gate insulating layer has an opening which follows an outer circumference of the pixel electrode, the opening being formed by removing the gate insulating layer.

2. The thin film transistor array panel of claim 1, wherein the gate wire has a gate line, and a gate pad connected to an end of the gate line; and the gate insulating layer has a contact hole exposing the gate electrode.

3. The thin film transistor array panel of claim 2, further comprising a first supplementary gate pad formed on the gate insulating layer adjacent to the gate pad, and a connecting pattern connected to the gate pad through the first

contact hol and directly connected to the supplementary gate pad.

4. The thin film transistor array panel of claim 3, wherein the connecting pattern is made of the same material as the data line.

5 The thin film transistor array panel of claim 4, wherein the connecting pattern has a first opening exposing the supplementary gate pad.

6 The thin film transistor array panel of claim 2, further comprising a data pad connected to an end of the data line, and a supplementary data pad formed under the data pad,

wherein the data pad has a second opening exposing the supplementary data pad.

7 The thin film transistor array panel of claim 2, further comprising a supplementary gate pad connected to the gate pad through the first contact hole, the supplementary gate pad being made of the same material as the data line; and a data pad connected to the end of the data line.

8. The thin film transistor array panel of claim 7, further comprising a passivation layer covering the data line, the data pad and the supplementary gate pad,

wherein the passivation layer has contact holes exposing the data pad and the supplementary gate pad, respectively.

9. A manufacturing method of a thin film transistor array panel comprising the steps of:

forming a gate wire including a gate line, a gate electrode, and a gate pad on an insulating substrate:

forming a gate insulating layer cov ring the gat wire;

depositing a semiconductor material on the gate insulating layer;

forming a semiconductor pattern on the gate insulating layer of the gate electrode by patterning the semiconductor material;

depositing a transparent conductive material on the gate insulating layer;

forming a pixel electrode by etching the transparent conductive material; and

forming an opening to remove a remaining conductive material, the opening being formed at a circumference of the pixel electrode.

10. The method of claim 9 further comprising the step of forming a first contact hole exposing the gate pad by dry etching the gate insulating layer.

11. The method of claim 10, further comprising the step of dry etching to remove a remaining transparent conductive material formed when forming the pixel electrode, this dry etching step being performed before or after dry etching the gate insulating layer.

12. The method of claim 9, further comprising the steps of:

depositing a data conductor on the gate insulating layer having the pixel electrode;

patterning the data conductor to form a data line, a source electrode, a drain electrode, a data pad, and a connecting pattern connected to the gate pad through the first contact hole;

depositing a passivation layer; and

patterning the passivation layer to form a first opening exposing the

connecting pattern and a second opening exposing the data pad.

13. The method of claim 12, further comprising the step of:

forming a supplementary gate pad under the connecting pattern and a supplementary data pad under the data pad when etching the transparent conductive material,

wherein the supplementary gate pad and the supplementary data pad are exposed through the first and the second openings, respectively.

14. A thin film transistor array panel for a liquid crystal display comprising:

a gate line formed in a horizontal direction on the insulating substrate;

a gate insulating layer covering the gate line;

a data line formed in a vertical direction on the gate insulating layer;

an align pattern formed on the gate insulating layer and located on both sides of the data line;

~~a semiconductor pattern formed on the gate insulating layer;~~

a drain electrode formed on the semiconductor pattern;

a source electrode formed on the semiconductor pattern, the source electrode being separated from the drain electrode and connected to the data line;

a passivation layer covering the data line, the align pattern, the drain electrode, and the source electrode, and having a contact hole exposing the drain electrode; and

a pixel electrode formed on the passivation layer and connected to the

drain electrod through the contact hole.

15. The thin film transistor array panel of claim 14, further comprising ohmic contact layers formed between the source electrode and the semiconductor pattern, and between the drain electrode and the semiconductor pattern.

16. The thin film transistor array panel of claim 14, wherein the passivation layer and the gate insulating layer have an opening exposing the insulating substrate between the align pattern and the data line.

17. A thin film transistor array panel for a liquid crystal display comprising:

a gate line formed in a horizontal direction on the insulating substrate;

a gate insulating layer covering the gate line;

a data line formed in a vertical direction on the gate insulating layer;

an align pattern formed on the gate insulating layer and located on both sides of the data line;

a semiconductor pattern formed on the gate insulating layer;

a drain electrode formed on the semiconductor pattern;

a source electrode formed on the semiconductor pattern, the source electrode being separated from the drain electrode and connected to the data line;

a pixel electrode formed on the gate insulating layer and connected to the drain electrode and the align pattern; and

a passivation layer covering the data line, the align pattern, the drain

electrod , the source lectrode, and the pixel electrode.

18. A manufacturing method of a thin film transistor array panel for a liquid crystal display comprising the steps of:

forming a gate line on an insulating substrate;

depositing a gate insulating layer and a semiconductor layer;

forming a semiconductor pattern by patterning the semiconductor layer;

forming a data line, a source electrode, a drain electrode and a align pattern;

depositing a passivation layer;

patterning the passivation layer to form a contact hole exposing the drain electrode and an opening between the data line and the align pattern; and

forming a pixel electrode.

19. A manufacturing method of a thin film transistor array panel for a liquid crystal display comprising the steps of:

forming a gate a gate line on an insulating substrate;

depositing a gate insulating layer and a semiconductor layer;

forming a semiconductor pattern by patterning the semiconductor layer;

forming a data line, a source electrode, a drain electrode and a align pattern;

forming a pixel electrode covering portions of the align pattern and the drain electrode;

depositing a passivation layer; and

patterning the passivation layer to form a contact hole exposing the drain

electrod and an opening betwe n the data line and the align pattern.

20. A thin film transistor array panel for a liquid crystal display comprising:

a gate wire which is formed on an insulating layer and includes a gate line extended in a horizontal direction, and a gate electrode connected to the gate lines;

a gate insulating layer covering the gate wire;

a semiconductor pattern formed on the gate insulating layer;

a data wire, which is formed on the semiconductor pattern, the data wire including a data line extended in a vertical direction, a source electrode and a drain electrode separated from the source electrode and positioned opposite the source electrode with respect to the gate electrode;

an align pattern formed on the semiconductor pattern and located on both sides of the data line;

a passivation layer pattern covering the data wire and the align pattern, the passivation layer having a contact hole exposing the drain electrode and an opening between the data line and the align pattern; and

a pixel electrode formed opposite the drain electrode with respect to the passivation layer, the pixel electrode being connected to the drain electrode via the contact hole.

21. The thin film transistor array panel of claim 20, wherein portions of the pixel electrode and the align pattern overlap to each other.

22. The thin film transistor array panel of claim 20, wherein a distance

between th data line and a boundary of the pixel electrode adjacent to the data line is equal to or greater than a distance between the data line and a boundary of the align pattern adjacent to the data line.

23. The thin film transistor array panel of claim 20, wherein a portion of the align pattern is exposed through the opening.

24. The thin film transistor array panel of claim 23, wherein the pixel electrode is extended on the align pattern and connected to the align pattern.

25. The thin film transistor array panel of claim 24, wherein the opening is extended to the semiconductor pattern and the gate insulating layer, and the insulating substrate is exposed through the opening.

26. The thin film transistor array panel of claim 25, wherein the semiconductor pattern and the gate insulating layer are under-cut under the align pattern adjacent to the data line.

27. The thin film transistor array panel of claim 20, further comprising repair lines overlapping the portion of the data line and the both end portions of the align patterns, respectively, the repair lines being formed on the same layer as the ~ ıte wire.

28. The thin film transistor array panel of claim 20, further comprising a supplementary data line formed on the same layer as the data wire, the supplementary data line intersecting the gate line,

wherein both and portions of the supplementary data line are connected to the data line.

. The thin film transistor array panel of claim 29, further comprising a

supplementary data line formed on the same layer as the pixel electrode, the supplementary data line intersecting the gate line,

wherein both end portions of the supplementary data line overlap the data line.

29. The thin film transistor array panel of claim 28, wherein the gate line includes a first gate line and a second gate line, and a gate connecting portion interconnecting the first gate line and the second gate line.